

Call for Papers

IEEE Asian Solid-State Circuits Conference

A-SSCC 2026

Location: The Lin Hotel, Taichung, Taiwan

Date: November 1 – 4, 2026

<https://a-sscc2026.org/>

Sponsored by IEEE SSCS, IEEE Region-10 SSCS Chapters

<https://sscs.ieee.org/>

Conference Theme: **IC the Future of AI**

The IEEE A-SSCC 2026 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates will be available at the A-SSCC official website <http://www.asscc.org/> (or <https://www.a-sscc2026.org/>).

Paper Submission

Prospective authors are invited to submit **two-page** manuscripts, including figures, tables and references, to the official A-SSCC 2026 website. **The two-page submission could include one-page additional supplements with figures and figure captions. Supplementary figures should not be referred to in the text of the paper.** For further details, see the A-SSCC Website. Papers are solicited in the following categories:

Regular Session

- 1. Analog Circuits & Systems:** Amplifiers, comparators, switched capacitor circuits, continuous-time & discrete-time filters, voltage/current references; power converters and regulators, energy harvesting circuits and systems, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.
- 2. Data Converters:** Nyquist-rate and oversampling A/D, D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, innovative and emerging converter architectures, etc.
- 3. Digital Circuits & Systems:** Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation, power reduction and management for digital VLSI, variation and fault-tolerant circuits, digital ML and AI circuits, digital circuits and systems for automotive applications.
- 4. System Integration & Signal Processing Systems:** System-on-chip or 3D integration, microprocessors, network processors, baseband communication processing system & architectures, system-level power management; multimedia and recognition processing systems; cryptographic, security, ML and AI processors, neuromorphic circuits and systems; bio-medical/neural-network processors and sensor network systems, automotive processors.
- 5. Wireless:** Receivers/transmitters/transceivers for wireless systems; narrowband and ultra-wideband RF, millimeter-wave and terahertz circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas and wireless SiPs incorporating multiple chiplets.
- 6. Wireline:** Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication; high-speed, low power, and digital/system techniques for wireline communication; clock and data recovery circuits.
- 7. Emerging Technologies and Applications:** Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; artificial intelligence system; bio-medical/bio-electronics/bio-inspired chip design, body-area network; flexible and printable electronics; silicon photonics; smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; non-traditional computing for combinatorial optimization problems and cryogenic circuits and systems.
- 8. Memory:** Volatile and Non-volatile memory; new memory designs for 3D/2D architectures, emerging devices such as resistive-/phase change-/magnetic-/ferro-electric- memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, memory subsystem, computing in memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in self-test.
- 9. FPGA:** Novel algorithm and/or architecture for integrated circuits validated by FPGA implementation. The authors of accepted papers are required to participate in demo sessions.
- 10. Industry Program:** This special category accepts only papers based on state-of-the-art industrial products. Strong emphasis on systems realized by silicon chips is encouraged. The papers should cover architecture, circuits, process technology, packaging and testing, including characterization results, die and system photos, as well as product demos

Special Session

- 1. Demonstration Program:** Three demonstration sessions will be held during the Conference. Student Design Contest (SDC) and FPGA Demo will be presented by the authors of selected papers, and Industry Demo including Start-up Showcase will be offered by industry groups who voluntarily apply for participation without paper submission.
- 2. Special Program:** Diverse special programs including Educational Session, Panels, and Mini-Forums will be organized. In addition, other exciting joint programs such as Young Professionals and Women-in-Circuits (WiC) Joint Mentoring Session, Start-ups Forum, and IT Vision in Asia will be held during the Conference.

Papers related to integrated circuits for intelligent systems are highly solicited. Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, and SoC are included in the scope of the conference. Papers only describing CAD tools and CAD algorithms are not considered. Authors must follow detailed instruction provided within the "Authors" section of the website, including the Authors' Guide and Pre-Publication Policy. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Conference. Extended versions of selected papers from the Conference will be published in a Special Issue of the IEEE Journal of Solid-State Circuits and a Special Issue of the IEEE Solid-State Circuits Letters.

Important dates

Paper submission June 03, 2026, 20:00 (GMT) **Acceptance notification** August 8, 2026
Final paper submission August 31, 2026

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