Workshop Title: **RFSoC & PYNQ in Action: From 5G to Quantum and Beyond**

Developed & Presented by: **Robert Stewart, Andrew Maclellan, Marius Siauciulis, and Louise Crockett**

University of Strathclyde, Glasgow, Scotland, UK.

Date, time and venue: **09:00 – 12:00, Thursday 11th December, ED 417B**

Abstract

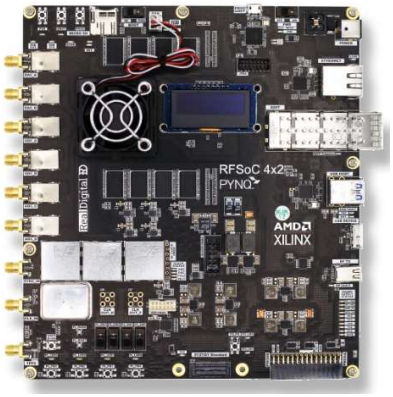
This workshop introduces a modern, application-driven approach to building high-performance radio systems using AMD's Radio Frequency System-on-Chip (RFSoC) technology. RFSoC devices combine FPGA fabric, application processor cores, and high-speed Radio Frequency (RF) data converters (DACs and ADCs), operating at multiple Gigasamples per second (Gsps) in a single chip, enabling high bandwidth and real-time operation directly at the edge.

This workshop focuses on how RFSoC-specific features can be used to build advanced wireless, sensing, and instrumentation, for applications like 5G communications and quantum. Through demonstrations and practical examples, we explore high-speed data capture techniques, FPGA-accelerated signal processing, and emerging workflows for deploying edge AI models and custom AI accelerators on RFSoC hardware. The workshop showcases end-to-end design strategies supported by the RFSoC-PYNQ framework, enabling researchers to rapidly prototype and evaluate complex RF systems.

Content Outline

The workshop intends to cover the following topics:

- An overview of RFSoC capabilities and how they enable modern RF applications.
- Review of the RFSoC-PYNQ development framework.
- Examples of application domains enabled by RFSoC-PYNQ.
- How to use the integrated RF Data Converters.
- Understanding the RFSoC clocking architecture.
- Outline of the design flow for RFSoC-based systems.
- Advanced concepts in high-speed data movement and intelligent processing.
- RFSoC for use-cases including 5G and quantum applications.
- Getting started: tools, resources, and community support.



Relevance to the FPGA Community

System on Chip (SoC) devices have come to the fore over recent years, with the combination of FPGA logic and capable processing systems in a combined platform proving compelling for many applications. AMD RFSoC devices are distinct among SoCs because they also incorporate multiple high-rate RF data converters; therefore they provide an ideal platform for developing programmable systems operating at the analogue/digital interface.

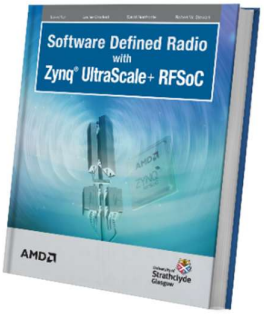
The drawback of SoC integration is that designing systems with these platforms can be complex. In this workshop, we use the RFSoC-PYNQ framework to explore a range of advanced ideas that support the development of modern, high-performance RF systems. The focus is on practical understanding while showing how the platform can be used to enable efficient and rapid experimentation. We also highlight tools, resources, and community materials that help attendees continue developing RFSoC-based applications beyond the workshop.

Format

The workshop will take the form of a 1/2 day technical short course, and will comprise lectures and demonstrations, with time for Q&A / discussion.

About StrathSDR

StrathSDR is the University of Strathclyde Software Defined Radio (SDR) research group.



In 2023, StrathSDR published a book "Software Defined Radio with Zynq UltraScale+ RFSoC", in collaboration with AMD. This book is available as a free PDF download from www.rfsocbook.com, as well as in paperback and hardback formats from Amazon and other retailers. It is accompanied by a downloadable set of practical materials and designs, featuring PYNQ.

The workshop is based on the expertise developed via this book and related research and development projects. We have also presented longer-form (3 day) courses on RFSoC development and complementary topics.

About the Workshop Team…

Brief biographies are as follows:

Robert (Bob) Stewart *(r.stewart@strath.ac.uk) is a Professor in the Department of Electronic Engineering, University of Strathclyde. He leads the 'StrathSDR' team, focusing on Software Defined Radio (SDR) and next generation radio access networks using shared spectrum with Dynamic Spectrum Access (DSA). Bob has led a number of 5G testbed and trials projects, and in recent years, his interests have included the development of solutions for the media and broadcast industry with private 5G SA networks, working alongside a number of international broadcasters. Over a 30 year career so far, Bob has published 4 books and more than 200 papers and has presented many industry short courses, including at UCLA Extension in the USA. Bob is also a director of University start-up company, Neutral Wireless Ltd.*

Andrew Maclellan *(a.maclellan@strath.ac.uk) received his MEng degree (distinction) in 2018, and PhD in 2025, both in Electronic and Electrical Engineering from the University of Strathclyde, Glasgow, Scotland. He is currently a Research Associate in StrathSDR, working in flexible radio design using AMD RFSoC devices. His primary research interests include Deep Learning for PHY layer wireless communications, with a specific interest in inference on the AMD RFSoC. Previously, Andrew interned in the Wireless HDL Toolbox team at MathWorks in Glasgow on three separate projects, and in 2020/21 he also interned with the PYNQ development team at Xilinx (now part of AMD).*

Marius Siauciulis *(marius.siauciulis@strath.ac.uk) is currently a Researcher in the StrathSDR team, while also writing up his PhD. Previously, Marius achieved a BEng (Hons) degree in Electrical and Electronic Engineering from the University of Strathclyde, graduating in 2019. His primary research interests include high speed data transfer to/from RFSoC devices, embedded systems development, and open source tooling for Software Defined Radio, including PYNQ and GNURadio. Marius has previously interned with MathWorks in Glasgow, and with Xilinx (now part of AMD), in both cases working in the areas of FPGA / SoC systems development and SDR.*

Louise Crockett *(louise.crockett@strath.ac.uk) was awarded MEng (distinction) and PhD degrees in Electronic and Electrical Engineering from the University of Strathclyde in 2003 and 2008, respectively. She is currently a Senior Lecturer and member of the StrathSDR research team, where she supervises / manages researchers and key sponsored projects. Her core research interests are in the implementation of DSP systems, FPGAs and SoCs, wireless communications, and SDR. Louise has previously co-authored three books on Xilinx/AMD technology. Her teaching focuses on digital systems design targeting FPGAs and SoCs, and builds practical skills to equip graduates for roles in industry.*