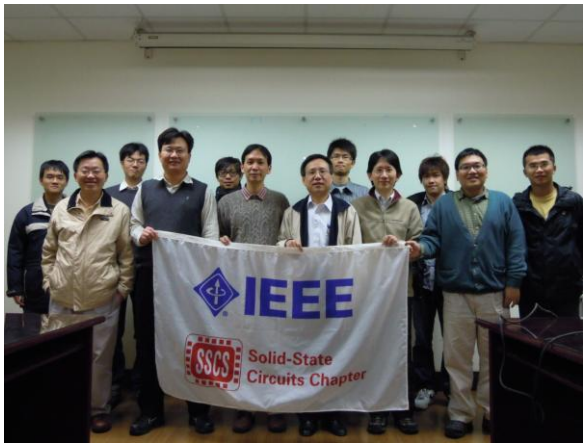
IEEE Taipei Section Newsletter

1. 2011 ISSCC Paper Rehearsal (Date: 2011.01.28)

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency and to network with leading experts.

According to instructions of ISSCC LRPC(Long Range Planning Committee) and FETC(Far East Technical Committee), speaker's rehearsal is especially important for all the speakers to attend to maintain its prestigious quality. The SSCS Taipei Chapter hosted a speaker's rehearsal for the papers from Taiwan to be presented at ISSCC 2011.

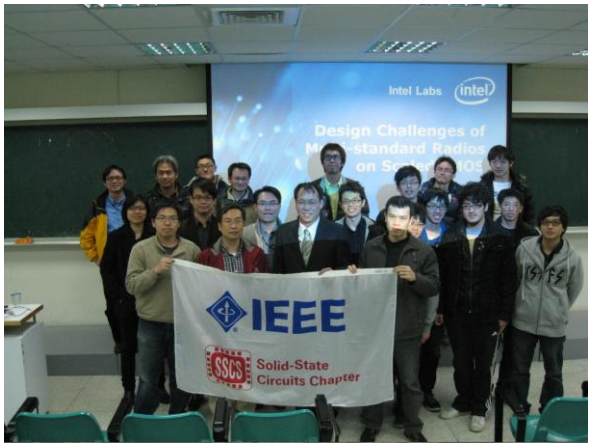


2. Design Challenges of Multi-Standard Radios on Scaled CMOS (Date: 2011.03.23)

Wireless technologies have become the fundamental elements in today's life. With the advance in CMOS technology and many proposed novel wireless circuit techniques, this trend is further pushed to a foreseeable versatile life style in the future with the affordable price. This talk exactly aims for the goal and presents two key techniques which are digital-assisted RF system and reconfigurealbe multi-standard radios. Because of this prospective study, not only students but many friends from industry also attend this seminar.

The key points of this talk are summarized as followed. Dr. Fu starts the talk from the aspect of cost for realizing a radio system. He uses Intel SOC Tick-Tock Model to clearly illustrate the signifincancy and necessarity of theses two key techniques and the importance of integration with digial circuits. Opportunities and challenges of theses two techniques are also given, including requirement of high linear front-end, high dynamic range data converter, low phase noise signal source, low out-of-band emission, regulation, and good isolation. He also talks about that combining digital techniques can provide many advantages, including digital calibration, realizing analog chip and digital chip in SOC, increasing the scability, speeding up the time to market. Dr. Fu then presents reconfigurable digital transmitter architecture that does not need front-end module. This architecture can be digitally controlled and support multi-standard application. Moreover, Dr. Fu also presents three novel circuit designs in Intel pusblished in the topest circuit design confirence, ISSCC and ESSCIRC, including a 2.5 GHz LNA integrated T/R switch, a 2.5 GHz high linear class AB PA, and a 2.5 GHz class D

outphasing PA. This talk gives us chance to access the newest wireless techniques. We also gain valuable pracitcal experience during Q&A section.



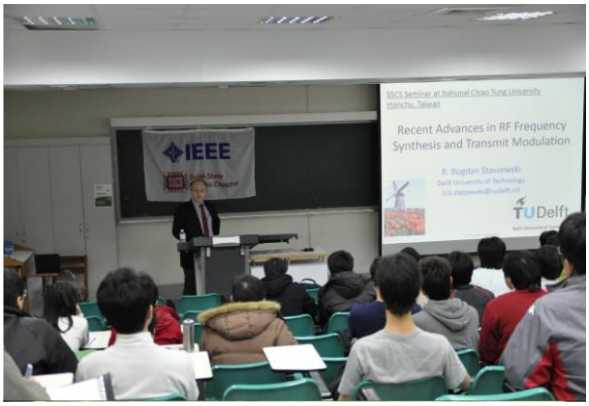
3. Recent Advances in RF Frequency Synthesis and Transmit Modulation

(Date: 2011.03.30)

Dr. Staszewski introduced some advance research studies on RF frequency synthsis and transmit modulation. As the VLSI technologies advance to the nano-meter CMOS arena, all-digital phase-locked loop (ADPLL) frequency synthesizers have drawn tremendous research efforts recently. Conventional charge-pump based analog PLLs suffer from lots of problem, including loop filter leakage, charge-pump distortions and reference spurs. Compare to conventional structures, ADPLL not only circumvents all above design issues, but also ideally realize true phase domain operation.

In a highly-scaled CMOS technology, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals, and the time-domain resolution can even reach to 20 ps in 40-nm CMOS. Since highly resolution can be easily achieved, constructing an ideal phase-domain operation becomes possible. The integer phase error is easily calculated by detecting the rising edges of the ideal reference phase and the actual measured variable phase, and then subtracting the phase results. The fractional phae error is detected by time-to-digital converter (TDC), including an inverter chain, a series of resampling DFF, parallel-thermometer-code detector, and a normalizer.

The most important design, the oscillator, can be digitally realized because of the tremendous progress of CMOS technology. The smallest size of varactor provides only tens of atto-farad capacitance, so a large linear varactor in conventional VCO is replaced with a large number of tiny binary-controlled varactors in a digitally-controlled oscillator (DCO). The LC-tank based oscillator has 4 tuning banks, including PVT, acquisition, tracking integer, and tracking fraction, and the frequency resolution of each bank is 4 MHz, 200 kHz, 12 kHz, and 12 kHz, respectively. In order to get higher frequency resolution, the tracking fraction bank is modulated by a 3rd order sigma-delta modulator(SDM), so, according to the dithering of the SDM, it breaks the periodicity for DCO static inputs which strongly reduces the reference spur issue. After that, Dr. Staszewski briefly introduced wide bandwidth ADPLL and software-defined PLL, and then ended the speech.



Prof. Sy-Yen Kuo

Chair, Taipei Section 2011